ABSTRACT OF THE DISCLOSURE

A memory mapped register file is disclosed for a data processing system that comprises a memory unit, input ports, and output ports. The memory unit includes a plurality of registers addresssable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode. The input ports receive inputs for addressing at least one register using an encoded address. The output ports output data from at least register addressable by an encoded address.

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